AMENDMENT

In The Claims:

Please amend the claims as follows:

Claim 1. (currently amended) A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside the CPU, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and synchronizing a plurality of blank periods of the display devices according to the common clock source, the plurality of blank periods of the display devices are in different frequencies;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process by the CPU during a non-responding period of the CPU, so as to reduce ~~a~~ consumptive power of the CPU, wherein memory access from the graphics-processing unit to the system memory through memory controller is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the blank periods of all display devices occur at the same time.

Claim 2. (previously presented) The method of claim 1, further comprising a step of detecting an upcoming least common multiple occurrence of the blank periods of the display

devices before the executing the power saving process.

Claim 3. (previously presented) The method of claim 1, wherein the blank periods can be a plurality of horizontal blank periods (HBPs).

Claim 4. (previously presented) The method of claim 3, wherein the horizontal blank periods are provided by the graphics-processing unit.

Claims 5 – 16 (cancelled)

Claim 17. (currently amended) A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside the CPU, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and synchronizing blank periods of the display devices according to the common clock source, the plurality of blank periods of the display devices are in different frequencies;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a CPU-clock rate and a power level of the CPU during a non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory through memory controller is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the

blank periods of all display devices occur at the same time.

Claim 18. (currently amended) The method of claim 17, wherein while executing the power saving process, the system memory is ~~continuously~~ accessed by the CPU during the non-responding period of the CPU.

Claim 19. (withdrawn) The method of claim 1, wherein the blank periods can be a plurality of vertical blank periods (VBPs).

Claim 20. (withdrawn) The method of claim 3, wherein the vertical blank periods are provided by the graphics-processing unit.